

## REMARKS

Entry of the above amendment and reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-7, 9-13, and 16 are pending in this application. Claims 1 and 9-13 are amended herein. Claim 16 is added herein. Claim 8 is cancelled herein.

Claim 8 is cancelled and replaced with claim 16 due to inconsistencies between the preamble (which directed the claim to forming a thin film resistor) and the limitations of the claim (which included forming both a thin film resistor and a plurality of metal lines).

The Examiner rejected claims 1 and 8 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 has been amended to clarify that the metal lines and resistor are physically separated from each other (as opposed to being formed separately). FIGs. 1, 2D-2F of the instant application clearly show 3 metal lines 70. Metal lines 70 are shown as the third metal interconnect level. Portions of metal lines 70 (e.g., the left two) serve as resistor contacts 64 and 66 (page 5, lines 10-14). The right most metal line 70 is physically separated from resistor 60. As described in the paragraph bridging pages 6 and 7, a mask 78 covers portions of the metal stack 76 where metal lines 70 are desired. The exposed portions of the metal stack 76 and resistor material 62 are then removed using a dry etch. The mask 76 is removed as the resulting structure is shown in FIG. 2D. The etching of metal stack 76 and resistor material 62 forms metal lines 70 including the right

most metal line 70 which is physically separated from the resistor. Furthermore, at page 7, lines 17-20, the specification teaches that the same metal stack used to form a metal interconnect level is used to form connections to the thin film resistor. Accordingly, Applicant respectfully submits that the subject matter of claim 1 is described in the specification in such a way so as to reasonably convey to one skilled in the art that the inventors has possession of the claimed invention. Applicant requests that the rejection be withdrawn.

The Examiner rejected claims 1 and 8 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter with applicant regards as the invention.

Applicant respectfully submits that claim 1 is amended to overcome the rejection. Claim 1 is amended to remove the term "thin film resistor area" and provide proper antecedent basis for the term "a thin film resistor". Accordingly, Applicant respectfully requests that the rejection be withdrawn.

The Examiner rejected claims 1-3, 7 under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ishii (U.S. 5,422,307).

Applicant respectfully submits that claim 1 is unanticipated by and patentable over Ishii as there is no disclosure or suggestion in Ishii of etching a metal stack and a layer of resistor material using a first pattern to form a plurality of metal lines and a thin film resistor, wherein the plurality of metal lines are physically separated from said thin film resistor. Ishii teaches forming a resistor by depositing a layer of resistor material and a metal stack, using a first pattern to etch the metal stack and resistor layer, and using a second pattern to etch the metal stack from over a high resistance area of the resistor layer. This leaves peripheral wiring at the ends of the resistor. There is no disclosure or suggestion in Ishii of forming a plurality of metal lines that are physically separated from the

thin film resistor. The only wiring taught by Ishii is the peripheral wiring of the resistor itself. No additional wiring is taught or suggested.

The Examiner argues that there is always more than one metal line formed during the fabrication of an integrated circuit so it would be obvious to form metal lines in addition to and separate from the thin film resistor area. Applicant admits that in a metal interconnect level multiple metal lines are typically formed. However, Ishii does not teach forming metal interconnects. Ishii teaches forming a resistor.

Conventionally, thin film resistors are formed using separate processing steps such that the resistors are located between metal interconnect levels. This is described in the Background of the Invention. In addition, references Ishikawa, Bailey, Morris, Linn, and Maghsoudnia all teach separate processing steps to form the thin film resistor versus forming the metal interconnects. Ishii is silent as to other structures that may be formed simultaneously with the resistor. There is nothing in Ishii to indicate a variation from the conventional concept of using one set of processes to form the thin film resistor and another set of processes to form any desired metal interconnect lines. There is no suggestion in the prior art for etching a stack of layers to form both a plurality of metal lines and a thin film resistor. While it may be possible to modify the pattern for the metal stack etch in Ishii to form both a thin film resistor and a plurality of metal lines, there is no suggestion to do so. In hindsight, after reviewing the Applicant's specification, it may be obvious to make the resistor of Ishii part of a metal interconnect level and have physically separated metal lines, but it is improper to use hindsight in rejecting the claims. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by and unobvious over Ishii.

The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Ishii as applied to claim 1, and further in view of Morris (U.S. 5,485,138).

Applicant respectfully submits that claim 6 is patentable for the reasons discussed above relative to claim 1, from which it depends.

The Examiner rejected claims 8-10, 12, 13 under 35 U.S.C. § 103(a) as being unpatentable over Ishii, Linn, and Morris. Claim 8 is cancelled. Claims 9, 10, 12, and 13 now ultimately depend from new claim 16 discussed below.

The Examiner rejected claims 4, 5, 11 under 35 U.S.C. § 103(a) as being unpatentable over Ishii or Ishii/Linn/Morris as applied to claims 1 and 8, and further in view of admitted prior art.

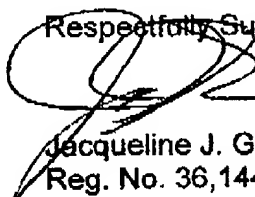
Applicant respectfully submits that claims 4 and 5 are patentable over the references for the same reasons discussed above relative to claim 1 from which these depend. Claim 11 now ultimately depends from claim 16 discussed below.

Applicant respectfully submits that newly added claim 16 is patentable over the references as there is no disclosure or suggestion in the references of dry etching a metal stack and a layer of resistor material using a first pattern to form at least one metal line and a thin film resistor, wherein the at least one metal line is physically separated from the thin film resistor. Accordingly, Applicant respectfully submits that claim 16 and the claims dependent thereon are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejection and allowance of claims 1-7, 9-13, and 16. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Texas Instruments Incorporated  
PO Box 655474, M/S 3999  
Dallas, TX 75265  
(214) 532-9348  
Fax: (972) 917-4418

Respectfully Submitted,



Jacqueline J. Garner  
Reg. No. 36,144

**RECEIVED**  
**CENTRAL FAX CENTER**  
SEP 12 2003

OFFICIAL